CpE 166  Advanced Logic Design
Computer Engineering
College of Engineering and Computer Science

Instructor: Dr. Jing Pang
Office: RVR 3008
Phone: 278-4549
Email: pangj@pajai.ecs.csus.edu
Office Hours: Tue, Th 12:00 p.m. -1:30 p.m.

Course Summary:
Present the advanced topics in digital logic design, including finite state machine designs, use of hardware description languages as a practical means to implement hybrid sequential and combinational designs, digital logic simulation, rapid prototyping techniques, metastability, hazards, races, testability, boundary scan, scan chains. VHDL and Verilog Hardware Description Languages are studied and used. Commercial Electronic Design Automation (EDA) tools and lab equipments are used to implement and test lab projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs).

Course Objectives:
1. Provide in-depth design experiences that require students to:
   a. develop good time management practices on their part
   b. develop problem solving skills
   c. meet design requirements and keep design within a resource limitation
   d. think creatively on complex assignments
   e. produce clear, concise written reports
   f. learn how to associate with others in the course, yet do individual work
2. Cover wide-ranging topics in logic design at an advanced technical level
3. Students to become proficient in the use of high-level design tools

Course Outcomes:
Students will design systems based on logic that includes multiple, interlocked state machines
Students will understand 'synthesis' and technology when using high level design tools (HDLs)
Students will acquire extensive hands-on laboratory skills
Students will design implementations for applications using SRAM, Flash memory, ADC, synchronization, Displays, Keypads (typical consumer, home, industry, etc. applications)
Students will write a technical, grammatically correct report
Students will demonstrate an understanding of ethics, need for life-long learning, and contemporary issues

Prerequisite:
• Completing CpE64, an introduction to logic design course
• Completing Engr 17, a basic circuit theory course

Textbook:
VHDL Design Representation and Synthesis, 2/E
by James R. Armstrong, F. Gail Gray
Publisher: Prentice Hall PTR
Copyright: 2000
ISBN: 0-13-021670-4

References:
Verilog HDL, 2nd edition
by Samir Palnitkar
Publisher: Prentice Hall, 2003
ISBN: 0130449113

HDL Chip Design
by Douglas J. Smith
Grades, Exams and Laboratory:

There will be two midterms and a final, each worth 100 points. Projects and reports will be worth 200 points. You must do satisfactory work in the lab to pass the course!

Course Policy:

1. Lecture attendance is required. If attendance becomes a problem quizzes will be given!
2. Project report late for one day will result in 5 points grade deduction. Project report late for two weeks will not be accepted.
3. You can not do project assignment in just three hours per week in the lab. It may take two or three times longer.
   The lab for this course is available all week. You are welcome to come to lab to work on your project including weekends whenever there are no other classes in the lab. Whenever you are in the lab, you need to consider yourselves ‘guardians’ of the workstations and equipments. When you use soldering lab, remember to clean the table and turn off the power of the soldering iron after you use them when you leave. Please don’t eat or drink in the lab. If the door is propped open and you are the last person to leave, turn off the lights and close the door behind you. If you see someone mistreating equipment, call campus security!
4. You are not allowed to use computers and PDAs in the exam.
5. You are required to submit an independent solution for each lab assignment. However, you may discuss assignments with your classmates but you must submit a separate and independent solution. For Policy on Academic Integrity, refer to: http://www.csus.edu/admbus/umanual/UMA00150.htm
CpE 166  Advanced Logic Design  Required Course

Course Description:
Present the advanced topics in digital logic design, including finite state machine designs, use of hardware description languages as a practical means to implement hybrid sequential and combinational designs, digital logic simulation, rapid prototyping techniques, metastability, hazards, races, testability, boundary scan, scan chains. VHDL and Verilog Hardware Description Languages are studied and used. Commercial Electronic Design Automation (EDA) tools and lab equipments are used to implement and test lab projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs).

Prerequisite:
- Completing CpE64, an introduction to logic design course
- Completing Engr 17, a basic circuit theory course

Textbook:
VHDL Design Representation and Synthesis, 2/E
by James R. Armstrong, F. Gail Gray
Publisher: Prentice Hall PTR
Copyright: 2000
ISBN: 0-13-021670-4

References:
Verilog HDL, 2nd edition
by Samir Palnitkar
Publisher: Prentice Hall, 2003
ISBN: 0130449113

HDL Chip Design
by Douglas J. Smith
Publisher: Doone Publications, 1998
ISBN: 0965193438

Verilog Coding for Logic Synthesis
by Weng Fook Lee
Publisher: John Wiley & Sons, Inc., 2003
ISBN: 978-0-471-42976-0

Course Objectives:
1. Provide in-depth design experiences that require students to:
   a. develop good time management practices on their part
   b. develop problem solving skills
   c. meet design requirements and keep design within a resource limitation
   d. think creatively on complex assignments
   e. produce clear, concise written reports
   f. learn how to associate with others in the course, yet do individual work
2. Cover wide-ranging topics in logic design at an advanced technical level
3. Students to become proficient in the use of high-level design tools

Topics Covered:
1. State machine design: Mealy and Moore finite state machine, state diagram, state table, algorithmic state machine chart.
2. VHDL and Verilog: syntax, synthesis to real hardware, simulation and testbench.
3. CPLD and FPGA: Xilinx CPLD and FPGA examples of configurable logic block, input/output block, programmable routing matrix, routing resources, clock distribution, configuration.
4. Testing: JTAG boundary scan, hazards in logic design, races, use of logic analyzers.
5. Codes: error detection and correction schemes, CRC generation.
6. Devices: ADC, LCDs, SRAM, Flash, databus, address bus, data paths and controls.
7. Transmission line effect in logic design and termination.

Class Schedule:

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
<th>Text Pages</th>
</tr>
</thead>
</table>
| 1    | Course introduction; Verilog basic concepts; Datatflow modeling; Combinational circuit coding. | James’s book 1-8  
Samir’s book 3-8, 27-35, 89-108  
Douglas’s book 39-71, 133-159 |
| 2    | Verilog behavioral modeling; D Flip-Flop with synchronous and asynchronous controls; Shift registers; Modeling of mixed sequential circuit with combinational circuit. | Samir’s book 119-166  
Douglas’s book 172-178 |
| 3    | Mealy and moore finite state machine, state diagram, state table, state encoding; SR latch debouncing circuit; Verilog structural modeling and hierarchical design method. | Samir’s book 330-331  
Douglas’s book 195-201, 3-25  
Samir’s book 51-52  
Samir’s book 11-25, 49-61 |
| 4    | Keypad circuit; Counter design with different control signals; Clock frequency divider design. | Handouts  
Samir’s book 110-112, 160  
Douglas’s book 163-171 |
| 5    | Midterm 1 review and midterm 1;                                                          |                                                |
| 6    | VHDL basics; VHDL hierarchical design; How LCD works; Hierarchical design interfacing with LCD display; Project #2 assigned. | James’s book 41-87, 99, 9-11  
Handouts |
| 7    | VHDL finite state machine; Algorithmic state machine chart.                            | James’s book 329-343  
Handouts |
| 8    | HDL coding for logic synthesis; Compare VHDL with Verilog. Midterm 2 review.            | James’s book 429-477  
Samir’s book 299-339  
Weng’s book 41-133  
Douglas’s book 133-217, 273-286 |
| 9    | Midterm 2; Bi-directional bus; SRAM and Flash memory address bus, data bus and controls; Project #3 assigned. | Handouts |
| 10   | Xilinx FPGA and CPLD architecture and configuration; Xilinx datasheet and web; Metastability. | Handouts |
| 11   | ADC data bus and controls; Interface FPGA with ADC.                                     | Handouts |
| 12   | Writing Testbench; Hazards and races.                                                   | James’s book 135-174, 489-530  
James’s book 299-307  
<table>
<thead>
<tr>
<th>13</th>
<th>JTAG, boundary scan, scan chains.</th>
<th>Handouts</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>Error detection and correction</td>
<td>Handouts,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Douglas’s book 179-192</td>
</tr>
<tr>
<td>15</td>
<td>Transmission line effect, active termination</td>
<td>Handouts</td>
</tr>
<tr>
<td>16</td>
<td>Final exam</td>
<td></td>
</tr>
</tbody>
</table>

**Laboratory Schedule:**

1. Project #1: (5 weeks)
   Coding and simulating combinational and sequential circuit, implement sequence detector and decode keypad.

2. Project #2: (5 weeks)
   Complex design with many interlocking hierarchical blocks, finite, state machines, and precise timing control for I/O devices.

3. Project #3: (5 weeks)
   Complex design centered on address bus, data bus, and controls for interfacing external memory chips and ADC chip. Testbench simulation of the data path and control of a simplified microprocessor model.

**Contribution of Course to Meeting the Professional Component:**

1. ABET category content as estimated by faculty member who prepared this course description:
   - Engineering science: 0.5 units or 12.5 %, Engineering design: 3.5 units or 87.5 %

2. The far ranging, complex designs assigned as projects provide the student with real world engineering design experiences. Students learn from others, improve problem solving skills, learn how to minimize resources, and manage their time.

**Course Outcomes:**

- **CpE 166 CO_1** Students will design systems based on logic that includes multiple, interlocked state machines
- **CpE 166 CO_2** Students will understand ‘synthesis’ and technology when using high level design tools (HDLs)
- **CpE 166 CO_3** Students will acquire extensive hands-on laboratory skills
- **CpE 166 CO_4** Students will design implementations for applications using SRAM, Flash memory, ADC, synchronization, Displays, Keypads (typical consumer, home, industry, etc. applications)
- **CpE 166 CO_5** Students will write a technical, grammatically correct report

**Relationship of Course Outcomes to Program Outcomes:** ABET designations, “a” through “k”

a. ability to apply knowledge of mathematics, science, and engineering – **CpE 166 CO_2 CO_4**
   Knowledge of electronics is required in the laboratory projects; students apply their knowledge of statistics when calculating mean time between failure, students use probability in one of their projects.

b. an ability to design and conduct experiments, as well as to analyze and interpret data – **CpE 166 CO_3**
   Logic analyzers collect signal data from actual hardware; students learn how to analyze and interpret what is, or is not, working properly – a major feature of this course.

c. an ability to design a system, a component, or process to meet desired needs – **CpE 166 CO_1 CO_4**
   The challenging projects have many design levels, requirements, and constraint limitations.

d. an ability to function on multi-disciplinary teams – **Not applicable.**

e. an ability to identify, formulate, and solve engineering problems – **CpE 166 CO_1**
   Projects #2 and #3 force students to formulate design diagrams and processes that lead to design solutions.

f. an understanding of professional and ethical responsibility – **CpE 166 CO_5**
   Students are constantly reminded that consulting with one another is professional and done in industry, however, copying solutions is not ethical and is not tolerated in this course; written assignments dealing with ethics are made.

g. an ability to communicate effectively – **CpE 166 CO_5** The reports from Projects #1 and #2 are graded critically by the instructors and often returned for re-writes; students are advised to keep either Project #2 or #3 for their CpE Career Portfolio.

h. the broad education necessary to understand the impact of engineering solutions in a global and societal context –
Some of the projects over the years relate to common activities of our society (devices for homes, cars, etc).

i. a recognition of the need for, and an ability to engage in life long learning – CpE 166 CO_2

Instructors describe new technology solutions for old problems, encourage students to read broadly, work “out of the box”, and predict new technology that students should anticipate.

j. a knowledge of contemporary issues - CpE 166 CO_4

Instructors include lecture material on issues such as security, monitoring.

k. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

CpE 166 CO_2 CO_3 This course uses the most recent tools, equipment, and devices from industry (construction, testing, use of logic analyzers, universal programmers, download techniques).

Course Coordinator and Preparer of this Course Description: Professor Jing Pang, September 20, 2009