EEE 239 – Advanced VLSI Design-For-Test II

Prerequisites: EEE 166 or ENGR 181, CPE 151 and EEE 238 **Date:** February 26, 2007

Course Area: Electrical and Electronic Engineering

Course Coordinator: Reed Linde

Catalog Description:

Memory-specific test methodologies and special features of memory designs employed in high volume manufacturing for improved testability, yield, and reliability are presented. Common memory design elements are studied, followed by the core SRAM, DRAM and NOR/NAND flash memory technologies. Other topics include memory test patterns and structural test methods, commonly used memory design-for-test techniques, and the application of ATD, redundancy, device trims, and error correction. 3 units.

Prerequisites: EEE 166 or ENGR 181, CPE 151 and EEE 238

Text: Information is conveyed primarily through instructor supplied notes. Various references from industrial and academic sources are also posted on WebCT, covering various related topics.

Additional Resources (optional, not required):

VLSI Memory Chip Design
Kiyoo Itoh
Springer Series in Advanced Microelectronics
Copyright 2001 by Springer-Verlag Berlin Heidelberg

High Performance Memory Testing
Design Principles, Fault Modeling, and Self-Test
R. Dean Adams
Kluwer Academic Publishers
Copyright 2003 by Kluwer Academic Publishers

Semiconductor Memories - Technology, Testing, and Reliability
Ashok K. Sharma
IEEE Press, Prentice Hall of India
Copyright 1997 by IEEE

Flash Memories
Paolo Cappelletti, et al.
Kluwer Academic Publishers
Copyright 1999 by Kluwer Academic Publishers, Third Printing 2001

Course Objectives:

This course is focused on the dominant VLSI memory technologies of SRAM, DRAM, and NOR/NAND flash, at the component level. Attributes of these technologies driving their market applications will be reviewed. Circuit elements common to these memory devices will be studied, including discussion of design/performance trade-offs, followed by review of the technology underlying the unit memory cell for each. Commonly used memory-specific test methodologies and design-for-test techniques will also be covered in detail, emphasizing their relation to specific common failure modes and reliability issues.

Prerequisites by Topic:

1. General undergraduate background in physics, chemistry, and DC/AC electronic circuits.
2. Semiconductor physics, including the theory of PN junctions and MOS transistor operation.
3. Analysis and design of CMOS combinational and sequential logic functions at the gate level.
4. Familiarity with VLSI manufacturing, fabrication techniques, failure modes, and test methods.
5. Basic probability theory and statistics (helpful, but not required)

Topics Covered:

1. Overview of VLSI memory technologies and their attributes and applications
2. General architecture and core technology of SRAM, DRAM and NOR/NAND flash memories
2. Goals, sensitivities, and methodologies of VLSI memory product manufacturing and test
3. VLSI memory product failure modes, test techniques and fault diagnosis approaches
4. VLSI memory product reliability modeling and qualification methodologies

Evaluation:

Homework is assigned periodically and due on specified dates prior to lecture. Typically five homework assignments are given in the semester.

There are two midterm exams and a cumulative final exam. Exams include conceptual questions as well as purely analytical questions. Exams are closed-book.

Each student is required to write a report on a topic related to VLSI memory product architecture, advanced VLSI memory technologies, memory testing and/or design-for-test methodologies, or memory manufacturing and qualification. Information for this research paper is derived from related industry and academic references. The paper requires 10 – 15 pages of student text.

The student's final grade is based on a point system, weighted according to the following:

Homework	15%
Midterm Exams	40%
Research Paper	20%
Final Exam	25%

Course Outline/Schedule

Week	*Topic*	*Text Reference*
1	Class Overview / Expectations / Logistics & MOS Memory Technology and Market Overview	Instructor Notes
2	Memory Product Architecture	Instructor Notes
3	Memory Product Architecture	Instructor Notes
4	Memory Product Architecture	Instructor Notes
5	SRAM Memory Technology	Instructor Notes
6	DRAM Memory Technology & RAM Test Methods	Instructor Notes
7	Review and Midterm #1	
8	RAM Test Methods	Instructor Notes
9	RAM Test Methods.	Instructor Notes
10	NOR Flash Memory Technology	Instructor Notes
11	NAND Flash Memory Technology	Instructor Notes
12	Review and Midterm #2	
13	Memory Failure Modes and Reliability Issues	Instructor Notes
14	Flash Memory Test Methods	Instructor Notes
15	Theory and Assessment of Product Reliability. Research Paper Due.	Instructor Notes
16	Final Exam	