

EEE 238 – Advanced VLSI Design-For-Test I

Prerequisites: EEE 166 or ENGR 181 and CPE 151

Date: February 26, 2007

Course Area: Electrical and Electronic Engineering

Course Coordinator: Reed Linde

Catalog Description:

Focus on integrated circuit design-for-test-techniques; semiconductor reliability factors and screening; semiconductor fabrication processes, device physics and related performance limitations; quantifying cost/quality tradeoffs; IC manufacturing flows and high-accuracy parametric test methods. 3 units.

Prerequisites: EEE 166 or ENGR 181 and CPE 151

Text: Information is conveyed primarily through instructor supplied notes. Various references from industrial and academic sources are also posted on WebCT, covering various related topics.

Additional Resources:

Introduction to VLSI Circuits and Systems (CPE 151 textbook ... recommended, but optional)

John P. Uyemura

John Wiley & Sons

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Course Objectives:

This course covers broadly the key elements of VLSI product development and manufacturing. It includes the high-level manufacturing flow, manufacturing economics and yield analysis, design-for-test methodologies, MOS silicon fabrication process basics, product performance and reliability, and logic tester architecture and test methodologies. The intent of the class is to provide students with a broad understanding of how the various elements of VLSI design, fabrication, and test interact, and how they are mutually optimized to create cost-competitive and reliable products.

Prerequisites by Topic:

1. General undergraduate background in physics, chemistry, and DC/AC electronic circuits.
2. Semiconductor physics, including the theory of PN junctions and MOS transistor operation.
3. Analysis and design of CMOS combinational and sequential logic functions at the gate level.
4. Basic probability theory and statistics (helpful, but not required)

Topics Covered:

1. Goals, sensitivities, and methodologies of VLSI product manufacturing and testing
2. Relationship between fabrication parameters and VLSI product performance and reliability
3. VLSI product test equipment, and product fault diagnosis and debug test techniques
4. VLSI product qualification methodologies

Evaluation:

Homework is assigned periodically and due on specified dates prior to lecture. Typically five homework assignments are given in the semester.

There are two midterm exams and a cumulative final exam. Exams include conceptual questions as well as purely analytical questions. Exams are closed-book.

Each student is required to write a report on a topic related to some aspect of VLSI product testing, design-for-test, VLSI manufacturing, or VLSI product/process development. Information for this research paper is derived from related industry and academic references. The paper requires 10 – 15 pages of student text.

The student's final grade is based on a point system, weighted according to the following:

Homework	15%
Midterm Exams	40%
Research Paper	20%
Final Exam	25%

Course Outline/Schedule

<i>Week</i>	<i>Topic</i>	<i>Text Reference</i>
1	Class Overview / Expectations / Logistics	Instructor Notes
2	Integrated Circuit Manufacturing Flow	Instructor Notes
3	Economics of Manufacturing and Yields	Instructor Notes
4	Design for Test / Design for Manufacturability	Instructor Notes
5	Design for Test / Design for Manufacturability	Instructor Notes
6	Review and Midterm #1.	
7	VLSI Fabrication Overview	Instructor Notes & Student References
8	Device Physics and Performance/Reliability	Instructor Notes & Student References
9	Device Parametric Performance. Sources of Device Specifications.	Instructor Notes
10	Overview of VLSI Testing	Instructor Notes
11	Review and Midterm #2.	
12	ATE (Automatic Test Equipment) Hardware / Software	Instructor Notes
13	Device Test Software Development and Test Vector Generation	Instructor Notes
14	Calibration/Accuracy of Test Equipment and ATE Debug Tools	Instructor Notes
15	Integrated Circuit Quality and Reliability. Research Paper Due.	Instructor Notes
16	Final Exam	