COURSE DESCRIPTION

Department and Course Number:  CSC 273   Course Coordinator   Behnam S. Arad

Course Title: Hierarchical Digital Design Methodology   Total Credits:  3

Current Catalog Description:
Introduces advanced logic modeling, simulation, and synthesis techniques. Topics include modeling using Hardware Description Languages (HDL’s), Register Transfer Level (RTL) representation, high-level functional partitioning, functional verification and testing, computer-aided logic synthesis, logical verification and testing, timing and delay analysis, and automated place and route process. Also covers design with Application Specific Integrated Circuits (ASICs) and programmable logic. Cross-listed with EEE 273, and can be counted only once for credit. Prerequisite: CSc 205, CPE 64, or equivalent.

Textbooks:
1. HDL CHIP Design, Douglas Smith, Doone Publications.

References:
1. A VHDL Primer, J. Bhasker, Prentice Hall.
3. User manuals for simulation and synthesis tools from appropriate vendors.

Course Goals:
1. Introduce top-down and bottom up design methodologies for hierarchical digital logic systems;
2. Provide an overview of digital design with HDLs;
3. Familiarize students with the state of the art automated logic simulation and synthesis tools;
4. Cover advanced topics such as delay analysis and design for testability,

Prerequisites by Topic:
1. logic design.
2. basic programming techniques.

Major Topics Covered in the Course:
1. Basic signal and register timing and delay analysis
2. Digital design with hardware description languages
3. Hierarchical design flow
4. High-level functional partitioning
5. RTL representation
6. HDL modeling styles and techniques
7. Functional simulation and verification
8. Design for testability
9. Timing and delay analysis
10. Logic synthesis
Laboratory projects

Each student will work on several projects in various areas covering topics from advanced digital design, modeling and simulation using HDLs, and logic synthesis (10 weeks).

Estimate CSAB Category Content

<table>
<thead>
<tr>
<th>CORE</th>
<th>ADVANCED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Structures</td>
<td></td>
</tr>
<tr>
<td>Algorithms</td>
<td></td>
</tr>
<tr>
<td>Software Design</td>
<td></td>
</tr>
<tr>
<td>Computer Organization and Architecture</td>
<td>0.5</td>
</tr>
<tr>
<td>Concept of Programming Languages</td>
<td></td>
</tr>
</tbody>
</table>

Oral and Written Communications

No significant component

Social and Ethical Issues

No significant component

Theoretical Content

This is a graduate advanced digital design course covering basic principles of signal and register timing, hierarchical digital design, modeling and simulation using HDLs, and logic synthesis.

Analysis and Design

The course is designed to introduce analysis and design principles of advanced digital systems. Term projects are designed to enforce the analysis and design concepts introduced in class. All students are required to analyze the requirements specified in the projects for various aspects of advanced logic design including modeling, simulation and synthesis and to design detailed implementations meeting those requirements.

Rev. 5/13/2002