CpE 166 Advanced Logic Design   <u>Required Course</u>

<u>2000 -2002 Catalog Description</u>: Advanced Logic Design. VHDL and Verilog Hardware Description Languages are studied and used on the following advanced level logic design topics: synchronous state machines, asynchronous state machines, metastability, hazards, races, testability, boundary scan, scan chains, and built-in self-tests. Commercial Electronic Design Automation (EDA) toolsets are used to synthesize lab projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs). Post synthesis simulations by these same tools verify the design before implementation on rapid prototyping boards in the lab. Prerequisite: CpE 064, 4 units.

<u>Prerequisites</u>: Knowledge of logic design; Logic gates, Boolean algebra, Karnaugh maps, sequential circuits, state machine theory and design, timing analysis, PLD exposure, simulation, and use of a high level language tool

<u>Text</u>: Smith, Douglas, <u>HDL Chip Design</u>,   Doone Publications, 1996, ISBN 0-9651934-3-8,
<u>Additional Support Material</u>   MAXplusII, HDL design package, Altera Corporation, Ver 10.0

<u>Course Objectives</u>:

1. Provide in-depth design experiences that require students to:
   a. develop good time management practices on their part
   b. develop problem solving skills
   c. meet design requirements and keep design within a resource limitation
   d. think creatively on complex assignments
   e. produce clear, concise written reports
   f. learn how to associate with others in the course, yet do individual work
2. Cover wide-ranging topics in logic design at an advanced technical level
3. Students to become proficient in the use of high-level design tools including synthesis and simulation

<u>Topics Covered</u>:

1. State machine design: review of basics, self-clocking, algorithmic, interlocking state machines
2. VHDL: basics, simulation, synthesis to real hardware, test benches
3. FPGAs: architecture, implementation, configuration options, on-board memory, Altera or Xilinx examples
4. Testing: JTAG, boundary scan, chain scans, hazards in logic design, races, use of logic analyzers
6. Codes: error detection and correction schemes, CRC generation
7. Devices: ADC, LCDs, LCD drivers, memories, datapaths
8. Transmission line effect in logic design, active termination

<u>Class Schedule</u>:

Week	Topic	Text Pages
1	State machine review, self-clocking, Project #1assigned	3-25, 195-201
2	VHDL basics	39-71
3	Altera FPGA, VHDL continued, metastability	Altera datasheet/web, 133-159
4	Keypad VHDL example, register/latch VHDL designs	163-173
5	LCD and LCD driver, timing control, Project #2 assigned	datasheet handout
6	VHDL synthesis, simulations, asynchronous inputs	201-217, 273-286
7	VHDL design techniques, test benches, hazards	75-110
8	Review and midterm exam	
9	JTAG, boundary scan, scan chains	handouts, Altera app. note
10	Verilog review, comparison to VHDL, project #3 assigned	re-read 133-217, 273-286
11	Codes, error detection and correction, CRC	handouts, 179-192
12	Review and midterm exam	
13	Memory, datapath control, bi-directional, ADC	handouts
14	Basic computer architecture, pipelining	refer to Mano text
15	Transmission line effect, active termination	refer to Wakerly text
16	Final exam	

Laboratory Schedule:

1. Project #1: VHDL (5 weeks) Build prototyping board, implement sequence detector, and decode keypad.
2. Project #2: VHDL (five weeks) Complex design with many interlocking state machines, precise timing control for I/O devices, memory interface, IP (Mega Wizards), resource limited, and with consumer appeal.
4. Project #3: Verilog (five weeks) Second complex design centered on data busses, dataflow and a RISC CPU.

Contribution of Course to Meeting the Professional Component:

1. ABET category content as estimated by faculty member who prepared this course description:
   Engineering science: 0.5 units or 12.5 %, Engineering design: 3.5 units or 87.5 %
2. The far ranging, complex designs assigned as projects provide the student with real world engineering design experiences. Students learn from others, problem solve, learn how to minimize resources, and manage their time.

Course Outcomes:

CpE 166 CO_1 Students will design systems based on logic that includes multiple, interlocked state machines
CpE 166 CO_2 Students will understand 'synthesis' and technology when using high level design tools (HDLs)
CpE 166 CO_3 Students will acquire extensive hands-on laboratory skills
CpE 166 CO_4 Students will design implementations of error detection and correction, CRC, scan chains, ADC, synchronization, Displays, Keypads (typical consumer, home, industry, etc. applications)
CpE 166 CO_5 Students will write a technical, grammatically correct report

Relationship of Course Outcomes to Program Outcomes: ABET designations, "a" through "k"

a. ability to apply knowledge of mathematics, science, and engineering – **CpE 166 CO_2 CO_4**
   Knowledge of electronics is required in the laboratory projects; students apply their knowledge of statistics when calculating mean time between failure, students use probability in one of their projects.
b. an ability to design and conduct experiments, as well as to analyze and interpret data – **CpE 166 CO_3**
   Logic analyzers collect signal data from actual hardware; students learn how to analyze and interpret what is, or is not, working properly – a major feature of this course.
c. an ability to design a system, a component, or process to meet desired needs – **CpE 166 CO_1 CO_4**
   The challenging projects have many design levels, requirements, and constraint limitations.
d. an ability to function on multi-disciplinary teams – **Not applicable**.
e. an ability to identify, formulate, and solve engineering problems – **CpE 166 CO_1**
   Projects #2 and #3 force students to floorplan and formulate processes that lead to design solutions.
f. an understanding of professional and ethical responsibility – **CpE 166 CO_5**
   Students are constantly reminded that consulting with one another is professional and done in industry, however, copying solutions is not ethical and is not tolerated in this course; written assignments dealing with ethics are made.
g. an ability to communicate effectively – **CpE 166 CO_5 The reports from Projects #1 and #2 are graded critically by the instructors and often returned for re-writes; students are advised to keep either Project #2 or #3 for their CpE Career Portfolio.**
h. the broad education necessary to understand the impact of engineering solutions in a global and societal context – **CpE 166 CO_4 Some of the projects over the years relate to common activities of our society (secrecy, security, games, identification, devices for homes, cars, etc).**
i. a recognition of the need for, and an ability to engage in life long learning – **CpE 166 CO_2**
   Instructors describe new technology solutions for old problems, encourage students to read broadly, work "out of the box", and predict new technology that students should anticipate.
j. a knowledge of contemporary issues - **CpE 166 CO_4**
   Instructors include lecture material on issues such as security, safety, monitoring.
k. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice –**CpE 166 CO_ 2 CO_3 This course uses the most recent tools, equipment, and devices from industry (construction, testing, use of logic analyzers, universal programmers, download techniques).**

Course Coordinator and Preparer of this Course Description: Professor Ronald W. Becker, December 2, 2002